OC–3 Singlemode 9–Pin Duplex SC Transceivers

NOTE

All numerical values are in metric units [with U.S. customary units in brackets]. Dimensions are in millimeters [and inches]. Unless otherwise specified, dimensions have a tolerance of ±0.13 [.005] and angles have a tolerance of ±2° . Figures and illustrations are for identification only and are not drawn to scale.

1. INTRODUCTION

This specification covers recommendations for application of OC–3 Singlemode 9–Pin Duplex SC Transceivers used primarily in synchronous optical network/asynchronous transfer mode (SONET/ATM) OC–3 intermediate–reach applications. The transceiver consists of a transmitter and receiver for performing the electro–optic conversions between electrical positive emitter coupled logic (PECL) level signals and optical signals. The transmitter contains a 1300 nm Fabry–Perot laser and a custom laser driver integrated circuit. The receiver contains a preamplifier with a GaAs PIN photodiode followed by a limiting amplifier with PECL compatible logic outputs.

The transceiver operates from a single +5.0 Vdc power supply and is designed with DC coupled differential PECL compatible transmitter and receiver data inputs/outputs (I/O). Data can be transmitted and received by this transceiver over a pair of 62.5/125 µm multimode or 9/125 µm singlemode optical fibers. The optical interface is designed with an SC connector. The package for this transceiver is the multi–sourced 9–pin module.

When corresponding with personnel, use the terminology provided in this specification to facilitate your inquiries for information. Basic terms and features of this product are provided in Figure 1.

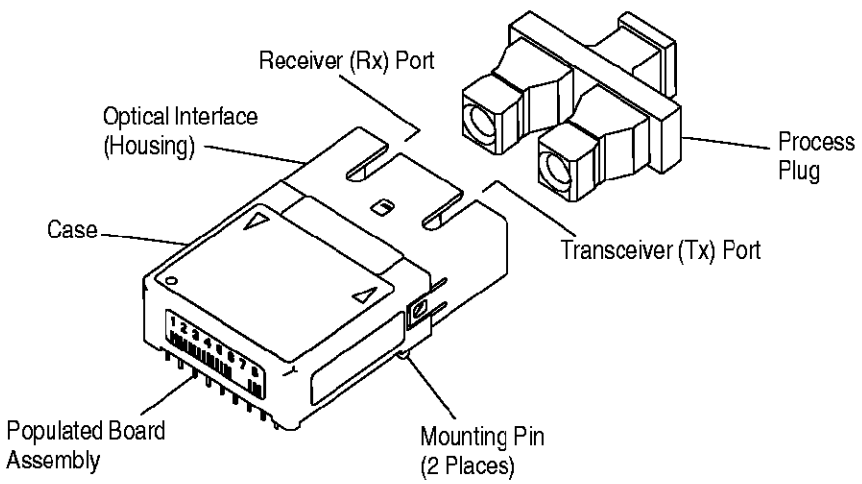


Figure 1

2. REFERENCE MATERIAL

2.1. Revision Summary

Per EC 0990–0264–03:

- Initial release of application specification

2.2. Customer Assistance

Reference Product Base Part Number 269085 and Product Code A466 are representative of OC–3 Singlemode 9–Pin Duplex SC Transceivers. Use of these numbers will identify the product line and expedite your inquiries through a service network established to help you obtain product and tooling information. Such information can be obtained through a local Representative (Field Service Engineer, Field Applications Engineer, etc.) or, after purchase, by calling PRODUCT INFO at the number at the bottom of this page.

2.3. Drawings

Customer Drawings for product part numbers are available from the service network. If there is a conflict between the information contained in the Customer Drawings and this specification or with any other technical documentation supplied, call PRODUCT INFO at the number at the bottom of page 1.

2.4. Instructional Material

Instruction Sheets (408–series) provide assembly instructions. Documents available which relate to this product are:

408–4212 Duplex Singlemode SC Connector Kits

2.5. Catalogs

Catalog 1307895 OC–3 Singlemode 9–Pin Duplex SC Transceivers

2.6. Standards and Publications

Standards and publications developed by the American National Standards Institute (ANSI), International Telecommunications Union–Telecommunications Standardization Sector (ITU–T), Telecommunications Industry Association and Electronic Industries Alliance (TIA/EIA), International Electrotechnical Commission (IEC), and Food and Drug Administration (FDA) provide industry test and performance requirements. Documents available which pertain to this product are:

ANSI T1.105.06, "Telecommunications: Synchronous Optical Network (SONET): Physical Layer Specifications"

ITU–T G.957, "Optical Interfaces for Equipments and Systems Relating to the Synchronous Digital Hierarchy"

TIA/EIA–455–95, "Absolute Optical Power Test for Optical Fibers and Cables"

TIA/EIA–526–4, "Optical Eye Pattern Measurement Procedure"

TIA/EIA–526–14, "Optical Power Loss Measurements of Installed Multimode Fiber Cable Plant—OFSTP 14A"

TIA/EIA–455–107, "FOTP 107—Determination of Component Reflectance or Link/System Return Loss using a Loss Test Set"

IEC 60825–1, "Part 1: Safety of Laser Products—Equipment Classification, Requirements and User's Guide"

IEC 60825–2, "Part 2: Safety of Optical Fibre Communication Systems"

FDA 21 Code of Federal Regulations (CFR) Chapter 1, Part 1040, "Performance Standards for Light Emitting Products"

NOTE

All products that contain a laser must comply with government regulations for laser safety. In the U.S., the applicable standard is FDA 21 CFR Chapter 1, Part 1040, and outside the U.S., IEC 60825–1 applies. These transceivers are designed and tested to meet the requirements of these standards and found to be in compliance with Class 1 laser safety limits. When operated within the limits specified in this document, this product conforms to IEC 60825–1: 1993 +A1: 1997 +A2: 2001, Class 1 laser product requirements.

2.7. Miscellaneous

Motorola DL140/D, "High Performance ECL Data Book, ECLinPs and ECLinPS Lite" provides a comprehensive description of transmission line design and termination techniques.

3. REQUIREMENTS

3.1. Laser Safety

These transceivers are designed and tested to be in compliance with Class 1 laser safety standards both in the U.S. and internationally when used within the limits specified in this document for temperature and power supply. These products are inherently safe since prolonged exposure to radiation from such lasers will not cause damage to the skin or eyes.

Laser safety is maintained during normal operation through factory–set adjustments which compensate for the known light of the laser versus current behavior as a function of temperature and power supply voltage. During single point failure conditions, laser safety is preserved by the internal optical subassembly which limits the emitted optical signal and ensures that even at the maximum light output of the laser, the accessible emission will not exceed Class 1 limits.

3.2. Assembly Precautions

Pc boards containing transceivers are normally tested to verify that the completed assemblies function correctly before they are shipped. Personnel handle large amounts of test cards, so the following precautions are appropriate:

- Electrostatic discharge (ESD) precautions, similar to those used in any modern electronic card, are recommended. Minimum recommended precautions include the use of a grounded wrist strap and a grounded conductive mat covering the work area.
- Fixtures should be designed such that the connector ferrules have as much play when inserted into a transceiver as they would if the connector were plugged in manually. An overly rigid blindmating to the transceiver under test can damage the device, connector, or both.
- Ferrules used in testers should be inspected, cleaned, and maintained regularly. Inspection should be done under sufficient magnification to detect microcracks in the fiber.

3.3. Function

The laser driver circuit accepts a digital logic level (PECL) input and provides the proper bias and modulation currents for maintaining the laser within its specified operating range. The receiver accepts an input from the fiber optic cable in the form of a modulated optical signal and converts it to a digital logic (PECL) output. This signal is focused onto a small area GaAs PIN photodiode which converts the incident light into a proportional photo–current. The transimpedance preamplifier converts the photocurrent into an analog voltage which is fed to the limiting amplifier (also referred to as a quantizer). The limiting amplifier converts the analog voltage into a digital logic signal that interfaces with external circuitry, such as a physical layer (PHY) chip. See Figure 2.

3.4. Signal Detect and Reference Generator

The signal detect circuit compares the signal from the quantizer with a reference generator to determine if sufficient signal–to–noise ratio exists for reliable signal reproduction. The output of this section is a logical flag, not an analog voltage. The signal is used as a rough link integrity monitor, not a bit error rate (BER) monitor. It is useful for recognizing when the input to the receiver has dropped well below recommended levels. The comparison is done with hysteresis so that the signal assert and deassert occur at different power levels. The difference between the assert and deassert levels provided by the hysteresis ensures chatter–free operation by preventing the signal from toggling between HIGH and LOW if the power levels hover around a certain point. The signal detect flag is a PECL output signal and should be connected to the controller chip with the appropriate termination and/or level translation circuit depending on the specific input requirements of the PHY chip.

3.5. Data Encoding and AC Coupling

PHY chips use an encoding scheme which is an advantagous way to transmit data using fiber optic transceivers. This encoding limits the run length (the number of consecutive 1s or 0s) and maintains DC balance by ensuring that, over time, an equal number of 1s and 0s are sent through the link. This is refered to as disparity neutral or balanced data.

Transceiver Functional Block Diagram

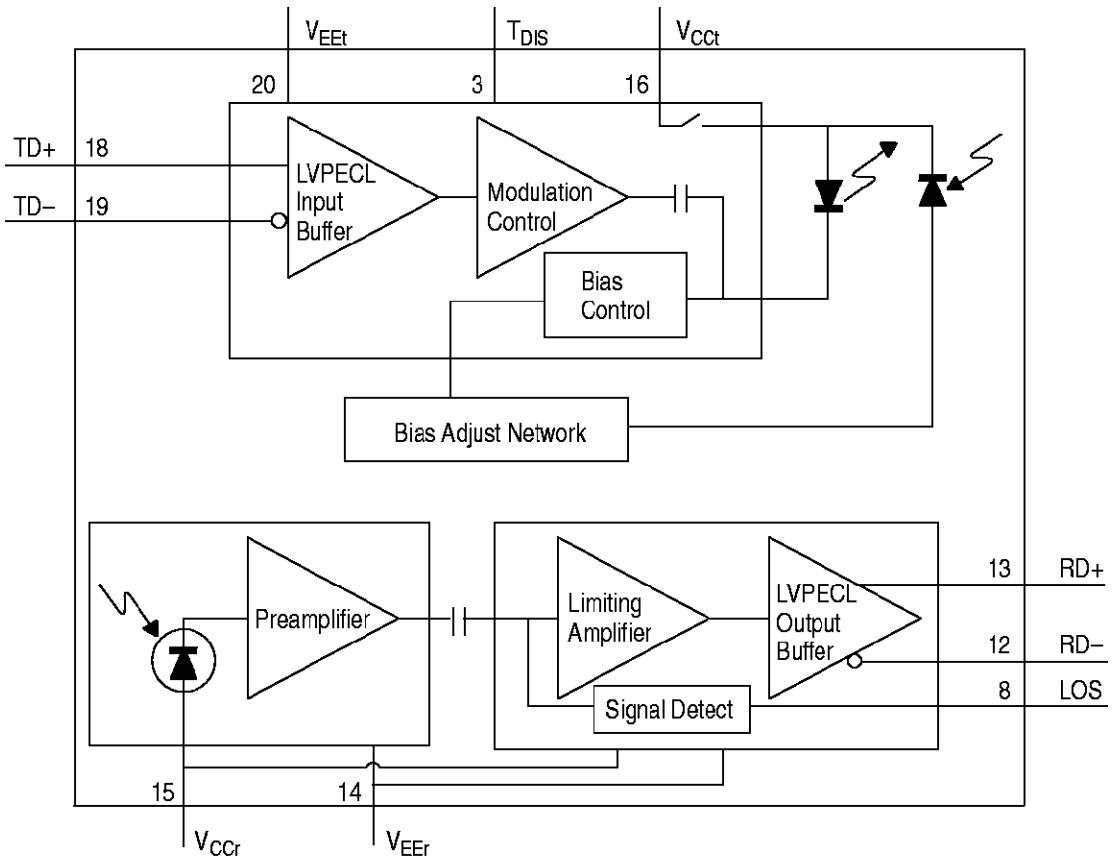


Figure 2

The receiver portion of the transceiver is internally AC coupled. Specifically, there are internal AC coupling capacitors in the data path between the preamplifier and post amplifier which control the lower 3 dB cutoff frequency of the receiver. This is done to limit the low frequency noise response of the receiver and improve sensitivity.

A direct result of AC coupling the receiver is that links, which use these transceivers, will not pass signals at DC or low frequencies. Long continuous strings of logic 1s or 0s, which have significant low frequency content, will be distorted by an AC coupled link. For this reason, the transceiver requires data to be encoded in a manner which limits the run length, such as asynchronous transfer mode/synchronous optical network (ATM/SONET) PRBS scrambling, etc. This is not a unique characteristic of these transceivers and is common for most commercially available fiber optic transceivers.

It is important to distinguish between an AC coupled transceiver as described, and an AC or DC coupled data interface which is described later. The electrical data interface at the receiver outputs and transmitter inputs can be either AC or DC coupled to the PHY integrated circuit depending upon the logic levels used, such as PECL, low voltage positive emitter coupled logic (LVPECL), etc. AC coupling is sometimes performed to provide translation between these logic levels, but is independent of the receiver internal AC coupling described. It is common to have an AC coupled transceiver that uses DC coupling to interface with the PHY chip I/O.

In most applications using optical transceivers, additional high speed circuitry, such as clock oscillators, is present on the application board. These high speed signals often lead to noise on power supply circuits at a high spectral bandwidth which can affect the performance of transceivers. Even though the transceivers provide electro–magnetic immunity regarding emission, ingress of radiation and immunity against conductive noise must be considered. Some basic recommendations are given in this document to assure optimum functionality.

When designing the electrical interface between the transceiver and the PHY chip, three key design goals must be addressed to achieve the best performance:

1. Terminate the transmission line with its characteristic impedance (typically 50 ohms).
2. Provide a DC current path for the PECL outputs to maintain the emitter follower outputs in the transistor active region.
3. Bias the PECL inputs at the middle operating point.

The transceiver PECL output drivers consist of a transistor configured as an emitter follower—making it is necessary to provide a DC current path through a resistive load. This creates a positive output current flow and ensures that the emitter followers are always sourcing current even with the +/– AC switching current necessary to drive the transmission line.

PECL inputs require the signal to be properly biased so that the DC offset is within the range of the input amplifier. A properly designed resistor network can serve the dual purpose of terminating the transmission line in its characteristic impedance and provide the necessary DC voltages to bias the PECL or LVPECL inputs and outputs. Specific circuitry for biasing the transceiver I/O is described later in this document.

The termination for PECL signals needs to be located at the input of the gate receiving the PECL signals which is at the end of the microstrip lines. Microstrip lines are recommended for optimum transmission signal quality. Termination recommendations are given for 50 ohm transmission lines. Recommended PCB layer structure is shown in Figure 3.

Recommended PC Board Layer Structure

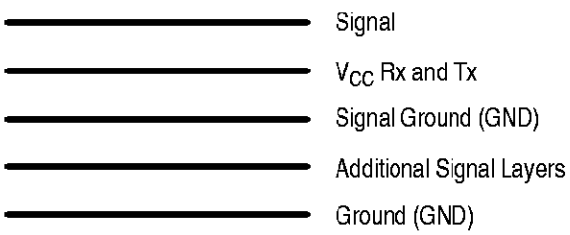


Figure 3

Connection to Vcc and GND should be done by vias to keep it as short as possible. GND islands should be tied to main GND by GND vias or should be avoided, if possible. Differential signal lines should be as short as possible and of equal length for timing/signal reasons. Transmitter data input lines and receiver data output lines should be kept far apart to prevent crosstalk. These lines can be run orthogonally or separated with a ground plane layer. One way to maintain the separation is to place all components for the transmit circuit on one side of the board and all components for the receive circuit on the other side of the board. Vias and layer changes should be avoided. The differential lines of each input or output stage should remain as close as possible using microstrip design rules.

3.6. Transceiver Filtering

Power supplies in the system must be adequately filtered to prevent supply noise from degrading transceiver performance. The theory behind commonly used power supply filtering techniques described in text books and integrated circuit data books is not covered in this document.

The recommended filter scheme separates the power supply to the transmitter and receiver. Power supply noise amplitude and frequency content is largely influenced by the type of supply used, high frequency logic and switching circuitry in the system, circuit board design, etc. For this reason, supply filter circuits should be evaluated under actual conditions before finalizing the design. Capacitors should be chosen with low effective series resistance, low dissipation factor and high Q. NPO or COG temperature characteristics are preferred because they provide more reliable performance over a wide range of environmental conditions. X7R types will also give acceptable performance; however, Y5V and Z5U should be avoided due to their large temperature and voltage coefficients. Ferrite beads used for L1 and L2 will provide higher noise attenuation because they do not possess the interwinding capacitance of a wound inductor. Refer to Figure 4.

Power Supply Filtering of the Transceiver

L1=L2=1 μH Note 1

C1, C3=0.01 μF to 0.1 μF Note 2

C2, C4=4.7 μF to 10 μF

Notes:

1 Ferrite beads could be used as an option

2 X7R or better MLC types are recommended for all capacitors

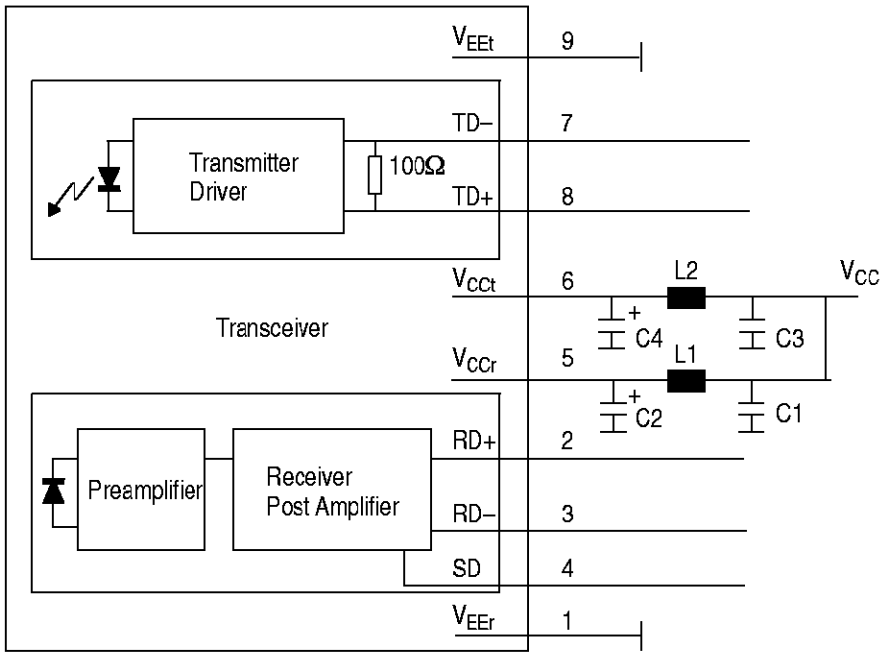


Figure 4

Small surface–mount packages are recommended since they exhibit less parasitic inductance which can lower the overall effectiveness of the bypass capacitor at high frequencies. Filter capacitors should be placed close to the transceiver power and ground pins to minimize noise coupling which can occur between the filter and the transceiver.

The impedance of power supply and ground lines on the pc board must be kept low. This is necessary because the dynamic current requirements of high speed digital circuitry can interact with a non–zero impedance to cause fluctuations in the voltage delivered to the transceiver. Therefore, this impedance leads to noise on the supply lines in addition to the inherent power supply switching noise. In order to keep the impedance low, the use of dedicated power and ground planes is strongly recommended.

3.7. Interfacing with PHY Integrated Circuits (ICs)

The transceiver is designed to be compatible with commercially available ICs. The majority of commercially available PHY chips operate from a single +3.3 V power supply but the transceiver is capable if interfacing with both +3.3 V and +5.0 V PHY chips if correctly configured. Generally, +3.3 V PHY chips use LVPECL compatible interfaces and +5.0 V PHY chips use PECL compatible interfaces for all high speed serial data I/O. Both LVPECL and PECL have a typical AC voltage swing of around 600 mV. For LVPECL, the AC signal is centered around 2.0 V. For PECL, the signal swings around a 3.7 Vdc level. Because of this difference in DC levels, AC coupling is necessary when interfacing between LVPECL and PECL I/O. Typical interface circuit examples are shown in Figures 5 and 6.

The transceiver is provided with differential data I/Os. It is not recommended to use this transceiver in a single–ended mode. Single–ended operation does not take advantage of the common mode noise rejection characteristics of the differential amplifier input stages. In many cases this results in reduced signal integrity, causes excessive electromagnetic interference (EMI) generation, and can compromise the performance of the transceiver. Possible interfaces for the transceiver are shown Figures 5 and 6.

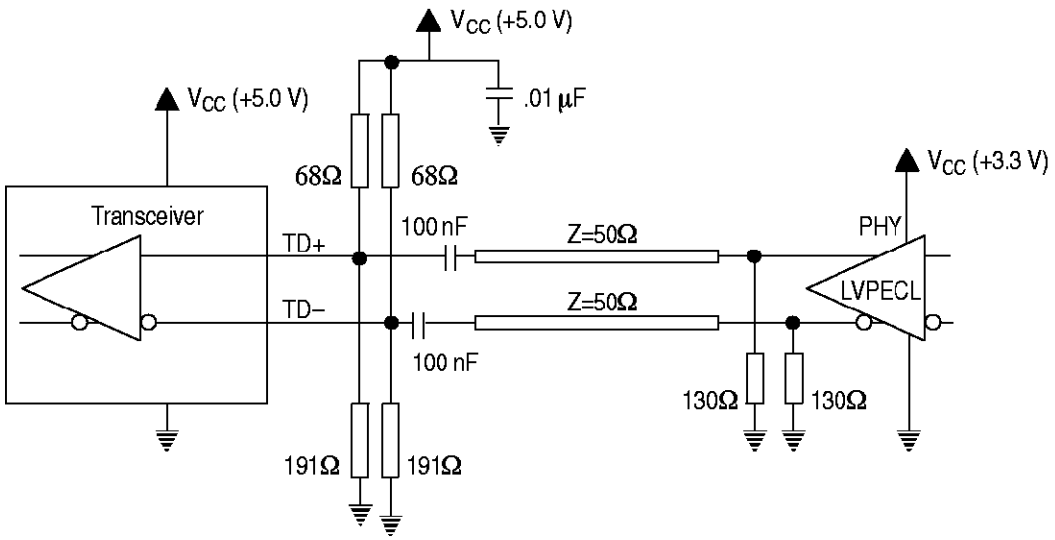
3.8. Soldering

A. Process

The transceiver is a through–hole device. The recommended method for soldering the transceivers to the pc board is wave soldering. Vapor–phase and reflow surface–mount processes are not recommended. Pins can be soldered at 240°C [464°F] for 10 seconds, provided the board adequately protects the case.

5.0 V Transceiver to 3.3 V PHY

Transmitter Interface



Receiver Interface

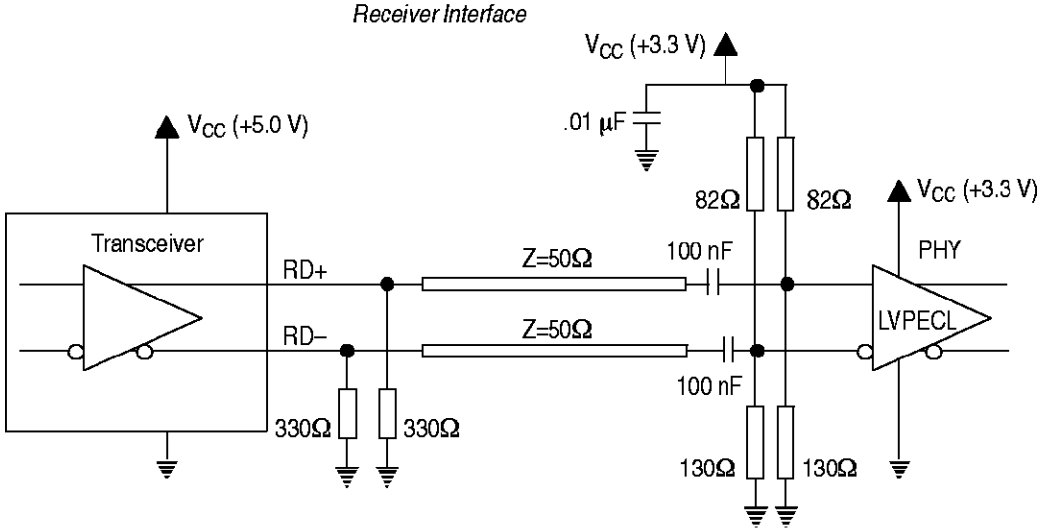


Figure 5

The recommended solder is a Type S composition containing 60% tin. The recommended flux is a water–soluble white rosin, Type S.

The transceiver is supplied with a process plug that is inserted into the optical interface. The plug protects the interface from contamination during soldering and cleaning. It is also a good idea to keep the plug installed during shipping and handling to prevent dust and dirt from entering the interface. Although the plug can emit air during a bubble leak test, this does not mean that the plug leaks and allows liquids or gases into the optical interface.

B. Cleaning and Drying

Pc boards should be cleaned with aqueous cleaners. Avoid solvents that could harm the polysulfone bodies of plastic–cased devices. The transceivers can be exposed to an air knife stream when being dried. On a drying rack, the optical interface should point down to ensure the best drainage away from the interface. If the plug is to be removed at that time, water must not be allowed into the interface. Water can leave a residue on the optics that will degrade the optical performance characteristics.

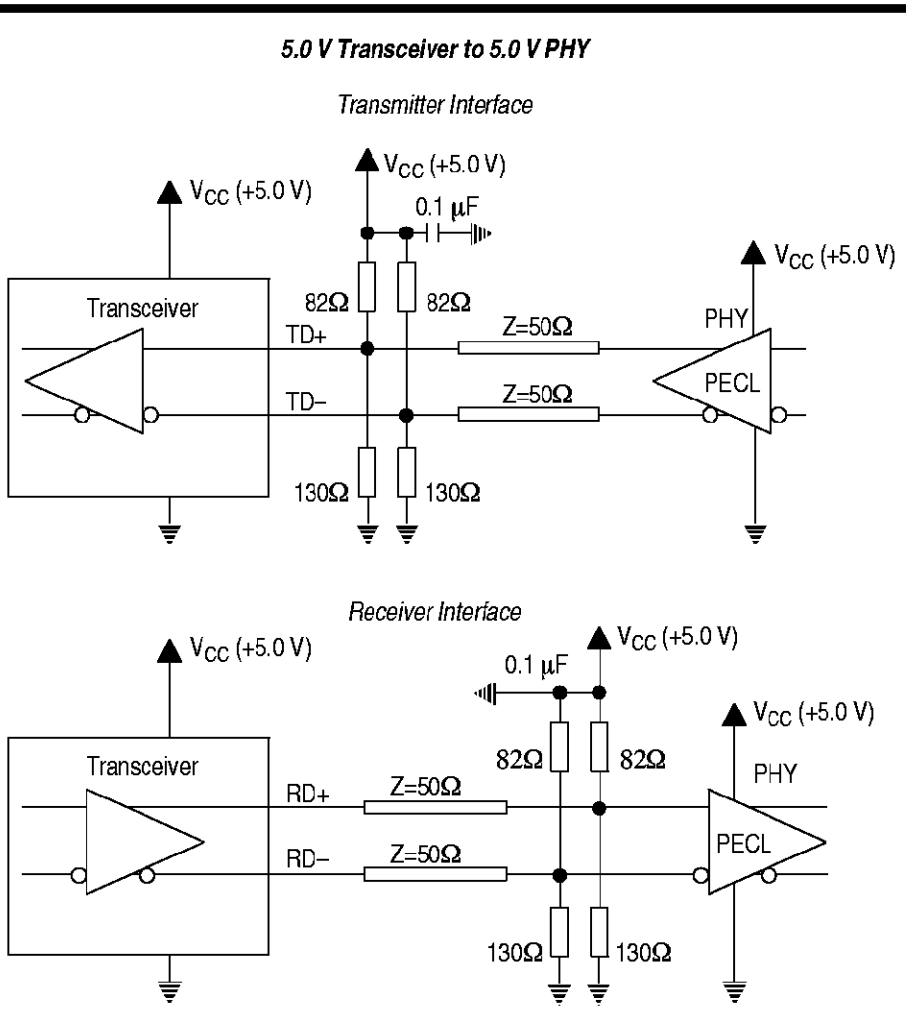


Figure 6

3.9. Cleaning the Optical Interface

Although the case of the transceiver is quite robust, care must be taken with the transceiver optics. Isopropyl alcohol is the only solvent that should be used to clean the transceiver. Filtered, dry air can be used to blow debris from the interface area. A grounded ESD–protected nozzle on the air hose must be used. Canned air can also be used; however, many cans contain additives in the air stream. These additives can leave a film on the optics.

Any procedures that could scratch the interface must be avoided. Any visible debris must be removed with a blast of air. It is recommended to flush the area rather than rub the lens with an alcohol–soaked swab. For stubborn or excessive dirt, the lens must be blasted with air, then flushed with alcohol, and blasted with air again.

3.10. Reliability

Fiber optic transceivers are considered high–reliability parts. Reliability applies not only to catastrophic failure of the part but also to its ability to transmit data reliably. There should be no bad data because of transceiver failure.

Fiber optic transceivers, like other semiconductor devices, follow the typical bathtub curve of reliability. For a typical batch of components, some parts will fail early—within the first few weeks or months of operation. This infant mortality stems from the inability of the parts to withstand the stresses of operation. After these parts have failed early in the life cycle, the remaining components will exhibit reliable, stable operation over many years. Eventually, after many years, some other parts will fail.

Early life failures can be caught during manufacturing and eliminated from shipped products by stressing component parts during manufacture and by burning in completed transceivers. The burn–in procedure involves temperature cycling the transceivers between the two extremes of –40°C and +85°C [–40°F and +185°F] for 13 cycles with a 30–minute dwell at each extreme. All component–level reliability procedures are based on Bellcore TA–NWT–000983.

The end of life (EOL) for an optical transceiver occurs when its operation degrades a defined amount. The amount of acceptable degradation before EOL depends on the application: 3.0 dB for telecommunication applications and 1.5 dB for data communication applications.

4. QUALIFICATION

A complete list of current qualifications cannot be maintained on this document; however, the following reference qualifications are representative of these transceivers. Qualification for specific transceiver part numbers can be obtained by contacting PRODUCT INFO at the number at the bottom of page 1.

Approved by Center for Devices and Radiological Health (CDRH) under Reference 9122051–03

Technischen Überwachungs–Vereine (TUV) Certificate R 9571032

5. TOOLING

No tooling is required for installing the transceiver.

6. VISUAL AID

Figure 7 shows a typical application of OC–3 Singlemode 9–Pin Duplex SC Transceivers. This illustration should be used by production personnel to ensure a correctly applied product. Applications which DO NOT appear correct should be inspected using the information in the preceding pages of this specification and in the instructional material shipped with the product or tooling.

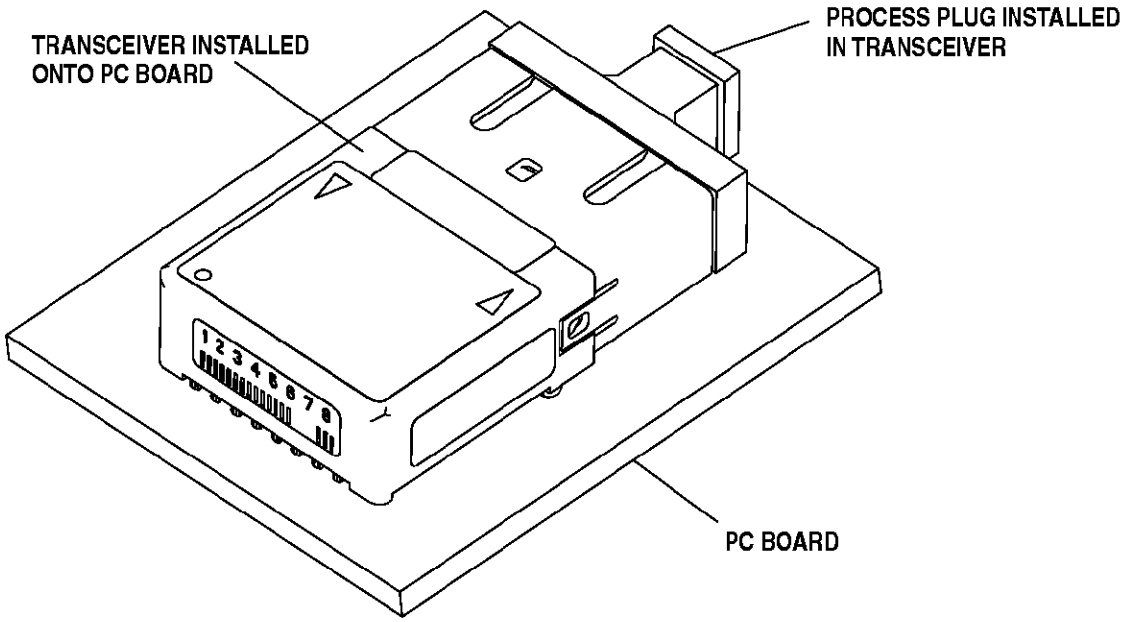


FIGURE 7. VISUAL AID